REMARKS

Claims 50-54 are pending in the present application. Claims 1-49 have been cancelled. Applicants note that in the Office Action dated June 16, 2004, claims 1-49 were listed as withdrawn from consideration. In the Preliminary Amendment filed with the application, claims 1-49 were cancelled. The listing of the claims starting on page 2 accurately lists these claims as cancelled.

In the Office Action dated June 16, 2004, the Examiner rejected claims 50-54 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Claims 50, 51, 53 and 54 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,237,441 to Nhu ("Nhu") in view of U.S. Patent No. 5,198,684 to Sudo ("Sudo"). Claim 52 was rejected under 35 U.S.C. 103(a) as being unpatentable over the Nhu reference and the Sudo reference as applied to claim 1 above, and further in view of U.S. Patent No. 5,200,631 to Austin et al. ("Austin").

Embodiments Disclosed in the Present Application

The embodiments disclosed in the present application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

An embodiment of the present application is illustrated in Figure 3. Referring to Figure 3, a chip 32 and a chip package 34 can transmit information to each other by using a set of converters capable of communicating with each other through the emission and reception of electromagnetic signals 42. Both the chip 32 and the chip package 34 have at least one such converter physically disposed on them. The chip 32 includes electronic circuitry 36 coupled to bonding pads 38 which, in turn, are coupled to first converters 40. Each first converter 40 receives a corresponding electric signal 41 from the circuitry 36 via the bonding pad 38, and converts the electric signal into an electromagnetic signal 42. The converter 40 then transmits the electromagnetic signal 42 to a corresponding second converter 44 located on the chip package 34. The second converter 44 receives the electromagnetic signal 42 and converts it to a

corresponding electric signal 45 that is applied to an inner lead 46 of the chip package. The various converters employed may transmit and receive electromagnetic signals over a wide range of frequencies, including visible light and infrared frequencies. Thus, not having a direct physical connection between the chip 32 and the chip package 34 decreases the inductive and capacitive effects commonly experienced with physical bonds, such as wire bonding, flip chip bonding, tape automated bonding, etc.

An embodiment disclosed in the present application directed to a memory device is shown in Figures 5 and 6. Referring to Figure 5, a memory device 99 including a semiconductor memory circuit 101 formed on a chip 100 and coupled to a chip package 102 through electromagnetic signals 104, 105, and 107 that include address, control, and data signals, respectively, for transferring data to and from the memory circuitry. The memory circuitry 101 includes an address decoder 106, a control circuit 108, and read/write circuitry 110. The address decoder 106, control circuit 108, and read/write circuitry 110 are all coupled to a memory cell array 112 and are also coupled to an address bus 114, a control bus 116, and a data bus 118 respectively.

The chip 100 includes an address converter 120 configured to receive electromagnetic address signals 104 and converts these signals into corresponding electric address signals that are applied to the address decoder 106 over the address bus 114. A control converter 122 of the chip 100 is configured to receive electromagnetic control signals 105 and converts these signals into corresponding electric control signals that are applied to the control circuit 108 over the control bus 116. A read/write converter 124 of the chip 100 operates during write operations of the memory device 99 to receive electromagnetic data signals 107 and convert these signals into corresponding electric data signals that are then applied to the read/write circuitry 110 over the data bus 118. The read/write converter 124 also operates during read data transfers of the memory device 99 to receive electric data signals on the data bus 118 and convert these signals into corresponding electromagnetic data signals 107. A package address decoder 126 is mounted on the chip package 102 adjacent the address decoder 106, and receives electric address signals 133 and converts these signals into the electromagnetic address signals 104, and a package control converter 128 mounted on the chip package adjacent the control converter 122 operates in the same way to generate the electromagnetic control signals 105 in response to electric control signals 132 applied to the chip package. A package read/write

converter 130 is mounted on the chip package 102 adjacent the converter 124 and operates during write operations to receive electric data signals 131 and generate the corresponding electromagnetic data signals 107. During read operations, the package read/write converter 130 receives the electromagnetic data signals 107 and generates the corresponding electric data signals 131. Thus, communication between the chip 100 and the chip package 102 is effected by transmitting electromagnetic data signals to and from the converters 120, 122, and 124 of the chip 100 with corresponding converters 126, 128, and 130 of the chip package 102.

Cited References

The Examiner has cited the Nhu reference. In Figures 3 and 4, the Nhu reference discloses a data processing module, wherein the communication between two microprocessor chips 10 mounted on a common electronic circuit board 20 is effected by optical signals. The chips 10 are interconnected through their terminal pairs 16-18′ and 18-16′ by optical fiber connectors 22 to which external connector terminals 24 and 26 are coupled. Each chip 10 includes a transceiver 12 and a logic microprocessor 14 operatively coupled to each other. Transceiver 12 includes data input terminal 16 and data output terminal 18 for receiving optical signals and an opposite pair of input and output terminals 16′ and 18′ for transmitting the optical signal as an electrical pulse. The circuit board 20 may also include components forming memory system 42 to which chips 10 are electrically coupled.

The Nhu reference does not disclose or fairly suggest that the circuit board 20 includes a converter that is operable to receive the data output electromagnetic waves from another converter and convert these received electromagnetic waves into corresponding electric data output signals that are applied to corresponding conductors, and the converter operable to receive electric address, data, and control signals on corresponding conductors and to convert these electric signals into corresponding address, data, and control electromagnetic waves that are communicated to the converter.

The Examiner has also cited the Sudo reference. The Sudo reference is directed to optically communicating between a plurality of semiconductor assemblies. As shown in Figures 1 and 2, a substrate 10 includes a silicon substrate 20, a predetermined number of semiconductor chips 30 flip chip mounted thereto on a center portion of the silicon substrate 20. The semiconductor chips 30 include solder bumps 65 that are electrically connected to the silicon

substrate 20. The substrate 10 also includes a light transmit-receive elements 40A and 40B disposed at openings at openings 50 provided on both sides of the center portion of the silicon substrate 20. The elements 40A and 40B respectively comprise photodiode chips 42A and 42B, and semiconductor laser chips 44A and 44B. As shown in Figures 1 and 2, a plurality of substrates 10 may be spaced apart and stacked together so that light transmit-receive elements 40A and 40B may optically communicate with each other.

The Sudo reference discloses that the semiconductor chips 30 are conventionally flip chip bonded to the silicon substrate 20 to enable communication therebetween. The Sudo reference does not disclose or fairly suggest effecting communication between the semiconductor chips 30 and the silicon substrate 20 by converting electromagnetic signals to electric signals. In fact, the Sudo reference teaches the opposite by disclosing flip chip type bonding between the silicon substrate and the semiconductor chips 30 which does not require any conversion of electromagnetic signals to electric signals or vice versa.

The Examiner has also cited the Austin reference purportedly to disclose transmitters that employ electromagnetic waves in the infrared spectrum.

Claim Rejections Under 35 U.S.C. 103(a)

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. The cited references do not teach or suggest all of the limitations of claim 50. Furthermore, there is no motivation or suggestion to combine the cited references to achieve the invention of claim 50.

Independent claim 50 recites, in part, "a chip package physically coupled to the chip, the chip package including a second converter that is operable to receive the data output electromagnetic waves from the first converter and convert these received electromagnetic waves into corresponding electric data output signals that are applied to corresponding conductors, and the second converter operable to receive electric address, data, and control signals on corresponding conductors and to convert these electric signals into corresponding address, data, and control electromagnetic waves that are communicated to the first converter." Neither the Nhu reference nor the Sudo reference teaches or suggests the above limitations. The Nhu reference appears to disclose that the microprocessor chips 10 and the memory system 42 are physically coupled to the electronic circuit board 20. However, the Nhu reference does not teach

or suggest the microprocessor chips 10 or the memory system 42 communicating with the electronic circuit board 20 using converters operable to perform the specific functions recited in claim 50. The Nhu reference is silent as to how the microprocessor chips 10 and the memory system 42 communicates with the electronic circuit board 20, but it appears to be conventional in operation. Similarly, the Sudo reference does not teach or suggest the semiconductor chips 30 communicating with the silicon substrate 20 using converters operable to perform the specific functions recited in claim 50. In fact, the Sudo reference teaches away by disclosing that communication between the semiconductor chip 30 and the silicon substrate 20 is effected by conventional flip chip solder bump bonding.

There is also no motivation or suggestion to combine the Nhu reference and the Sudo reference to achieve the present invention of claim 50. Any combination of the Nhu reference and the Sudo reference would result in employing the light transmit-receive elements 40A and 40B of the Sudo reference to enable communication between a plurality of electronic circuit boards 20 having respective microprocessor chips 10 thereon of the Nhu reference.

Claims depending from claim 50 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims.

Claim Rejections Under 35 U.S.C. 112

The Examiner has rejected claims 50-54 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Specifically, the Examiner asserts that the limitations of claim 50 "imply that the first converter converts the electric signal into [an] EM wave and at the same time converting EM waves back to the electric signal, and further, the converted EM waves being communicated to the first converter." (Office Action dated June 16, 2004, Pages 2-3). The limitations of claim 50, in part, define a memory device including a first converter *operable* to receive signals and *operable* to convert the signals to electromagnetic waves and vice versa. The limitations of claim 50 also require that the memory device include a chip package having a second converter *operable* to receive electromagnetic waves from the first converter and *operable* to convert these signals to electric signals and vice versa. Thus, the limitations of claim 50 define a computer system having a memory device including a chip

comprising a first converter operable to perform the specific operations recited in claim 50 and a chip package comprising a second converter which is also operable to perform the specific operations recited in claim 50.

The Examiner has also asserted that the limitations "address, data, and control electromagnetic waves" recited in claim 50 are indefinite. (Office Action dated June 16, 2004, Page 3). The above limitations refer to electromagnetic waves corresponding to address, data, and control signals from the chip package that are converted and transmitted respectively from the second converter to the first converter of the chip.

All of the claims remaining in the application (claims 50-54) are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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